What is claimed is:

1. A method for fabricating a capacitor for use in a semiconductor device, comprising the steps of:

forming a stack layer sequentially deposited in an order of an inter-layer insulation layer and a first etch barrier layer on a substrate, wherein a hole exposing a partial portion of the substrate passing through the inter-layer insulation layer and the first etch barrier layer is formed;

forming a storage node contact plug contacted to the partial portion of the substrate by being buried into the hole;

forming a storage node insulation layer on the stack layer, the storage node insulation layer having a concave pattern of which bottom region has a wider critical dimension (CD) than that of a top region and exposing the storage node contact plug;

forming a lower electrode inside of the concave pattern, the lower electrode being connected to the storage node contact plug; and

forming sequentially a dielectric layer and an upper electrode on the lower electrode.

2. The method as recited in claim 1, wherein the step of forming the storage node insulation layer having the concave pattern includes the steps of:

depositing a second etch barrier layer and a first

storage node insulation layer on the storage node contact plug to form a pillar-type pattern of which bottom region has a wider CD than that of a top region;

forming a second storage node insulation layer encompassing the pillar-type pattern; and

removing selectively the pillar-type pattern with use of the first etch barrier layer as an etch barrier layer to expose the storage node contact plug as simultaneously as to form a concave pattern having an inverted shape of the pillar-type pattern.

3. The method as recited in claim 2, wherein the step of forming the concave pattern by selectively removing the pillar-type pattern includes the steps of:

etching the first storage node insulation layer by using the second etch barrier layer as an etch barrier layer; and

etching the second etch barrier layer by using the first etch barrier layer as an etch barrier layer.

4. The method as recited in claim 3, wherein the first storage node insulation layer and the second etch barrier layer are etched through the use of a wet etching process.

5. The method as recited in claim 3, wherein the first storage node insulation layer is etched through the use of a wet etching process and the second etch barrier layer is etched through the use of a dry etching process.

6. The method as recited in claim 2, wherein the first storage node insulation layer and the first etch barrier layer are nitride layers and the second etch barrier layer is a polysilicon layer.

7. The method as recited in claim 2, wherein the first storage node insulation layer and the first etch barrier layer are nitride layers and the second etch barrier layer is a titanium nitride layer.

8. The method as recited in claim 6, wherein the first storage node insulation layer is proceeded with the wet etching process by using a solution of phosphoric acid (H_3PO_4), and the second etch barrier layer is proceeded with the wet etching process by using a mixture solution of nitric acid/hydrofluoric acid/ethanoic acid ($HNO_3/HF/CH_3COOH$).

9. The method as recited in claim 7, wherein the first storage node insulation layer is proceeded with the wet etching process by using a solution of H_3PO_4 and the second etch barrier layer is proceeded with the wet etching process by using a mixture solution of sulfuric acid/hydrogen peroxide (H_2SO_4/H_2O_2).

10. The method as recited in claim 1, wherein the step of forming the lower electrode further includes the step of nitridating a surface of the lower electrode.

11. A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming a stack layer by depositing sequentially an inter-layer insulation layer and a first etch barrier layer on a substrate;

forming a storage node contact hole exposing a partial portion of the substrate by etching the stack layer;

forming a storage node contact plug connected to the substrate by being buried into the storage node contact hole;

depositing a second etch barrier layer and a first storage node insulation layer on the storage node contact plug and the stack layer;

performing a dry etching process to the first storage node insulation layer and the second etch barrier layer to form a pillar-type pattern of which bottom region has a wider critical dimension (CD) than that of a top region on the storage node contact plug;

forming a second storage node insulation layer encompassing the pillar-type pattern;

removing selectively the pillar-type pattern to form a concave pattern exposing the storage node contact plug;

forming a lower electrode inside of the concave pattern, the lower electrode being connected to the storage node contact plug and having a wider critical dimension at its bottom region than at its top region; and

forming sequentially a dielectric layer and an upper electrode on the lower electrode.

12. The method as recited in claim 11, wherein the step of forming the concave pattern by selectively removing the pillar-type pattern includes the steps of:

etching the first storage node insulation layer with use of the second etch barrier layer as an etch barrier layer; and

etching the second etch barrier layer with use of the first etch barrier layer as an etch barrier.

13. The method as recited in claim 12, wherein the first storage node insulation layer and the second etch barrier layer are etched by employing a wet etching process.

14. The method as recited in claim 12, wherein the first storage node insulation layer is etched through the use of a wet etching process and the second etch barrier layer is etched through the use of a dry etching process.

15. The method as recited in claim 12, wherein the first storage node insulation layer and the first etch barrier layer are nitride layers and the second etch barrier layer is a polysilicon layer.

16. The method as recited in claim 2, wherein the first storage node insulation layer and the first etch barrier layer are nitride layers and the second etch barrier layer is a titanium nitride layer.

17. The method as recited in claim 15, wherein the first storage node insulation layer is proceeded with the wet etching process by using a solution of H_3PO_4, and the second etch barrier layer is proceeded with the wet etching process by using a mixture solution of $HNO_3/HF/CH_3COOH$.

18. The method as recited in claim 16, wherein the first storage node insulation layer is proceeded with the wet etching process by using a solution of H_3PO_4 and the second etch barrier layer is proceeded with the wet etching process by using a mixture solution of H_2SO_4/H_2O_2.